

Exhibit B

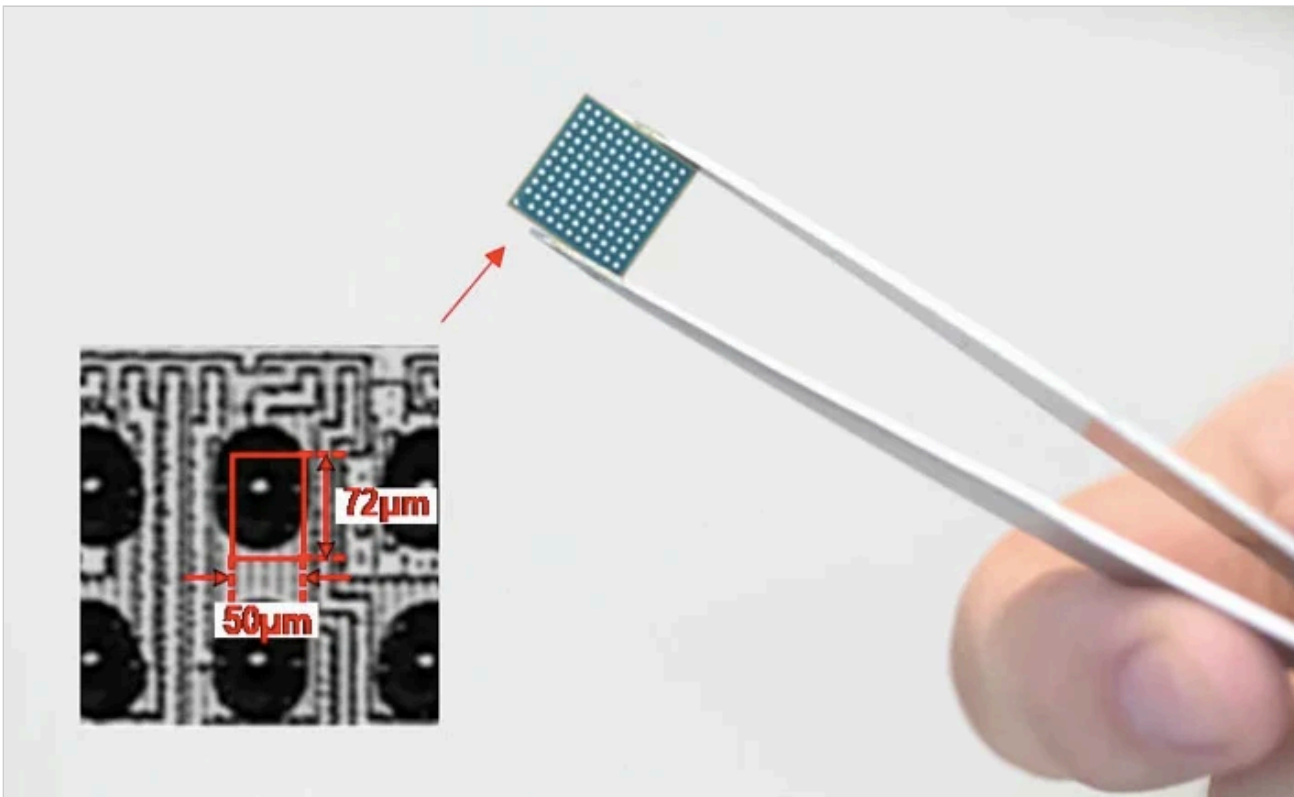
News

Researchers Create “World’s Smallest Digital PLL Circuit” for Next-Gen 5 nm Semiconductors

February 15, 2020 by [Cabe Atwell](#)

The scientists at the Tokyo Institute of Technology and Socionext Inc. have implemented PLLs (Phase-Locked Loop) in a 5-nm CMOS process using only digital standard cells.

Scientists from the Tokyo Institute of Technology and Socionext Inc. claim to have created the [world’s smallest all-digital PLL \(Phase-Locked Loop\) circuit](#), which kicks open the door to designing next-gen 5-nm semiconductors and paves the way for a new wave of digital technologies.



Chip containing the $50 \times 72 \mu\text{m}^2$ -sized PLL. Image used courtesy of [Tokyo Tech News](#)

PLLs and 5 nm

Manufacturers are currently looking at ways to develop increasingly smaller and more efficient semiconductors down to the 5-nm process—a significant improvement over the 7-nm process, which is currently in production.

Shrinking down to the 5-nm process would bring about faster and more efficient processors. However, getting there requires overcoming a key component—in this case, PLLs. PLLs refers to a control circuit that generates an output signal whose phase is related to the input phase signal.

PLLs are a critical circuit made up of several components (variable frequency oscillator, phase detector, and a feedback loop) that provide precisely timed clock pulses to digital logic circuits.

Those PLL components are analog, which are generally bulky and have designs that limit their scalability, meaning reducing them in size is quite the obstacle. That said, the scientists from Tokyo Tech and Socionext claim to have successfully overcome that obstacle by designing what they term a “synthesizable fractional-N PLL,” which replaces the analog components with digital logic gates, making it possible to produce semiconductors in the 5-nm range.

Reducing the Area of PLLs

The scientists, led by Professor Kenichi Okada, used several techniques to reduce the area size of the PLLs, along with their power consumption and jitter (unwanted time fluctuations while transmitting signals).

	This Work	TCAS-I'18 Shen	RFIC'18 Kim	ISSCC'15 Tsai	ISSCC'15 Song
Affiliation	Tokyo Tech & Socionext	Intel	Samsung	TSMC	Samsung
Synthesizable?	Yes	No	No	No	No
Process	5nm	14nm	14nm	16nm	14nm
Area [mm ²]	0.0036	0.021	0.1	0.029	0.009
Power Consumption[mW]	0.95	2.6	36.3	3.9	2.06
Jitter[ps]	1.90	15.1	0.982	3.48	18.8
FOM*[dB]	-234.7	-212.3	-224.6	-223.3	-211.4

$$*FOM = 10\log_{10} \left[\left(\frac{Jitter}{1s} \right)^2 \cdot \left(\frac{Power\ Consumption}{1mW} \right) \right]$$

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Performance comparison of PPLs in the sub-20nm process. Image used courtesy of [Tokyo Tech News](#)

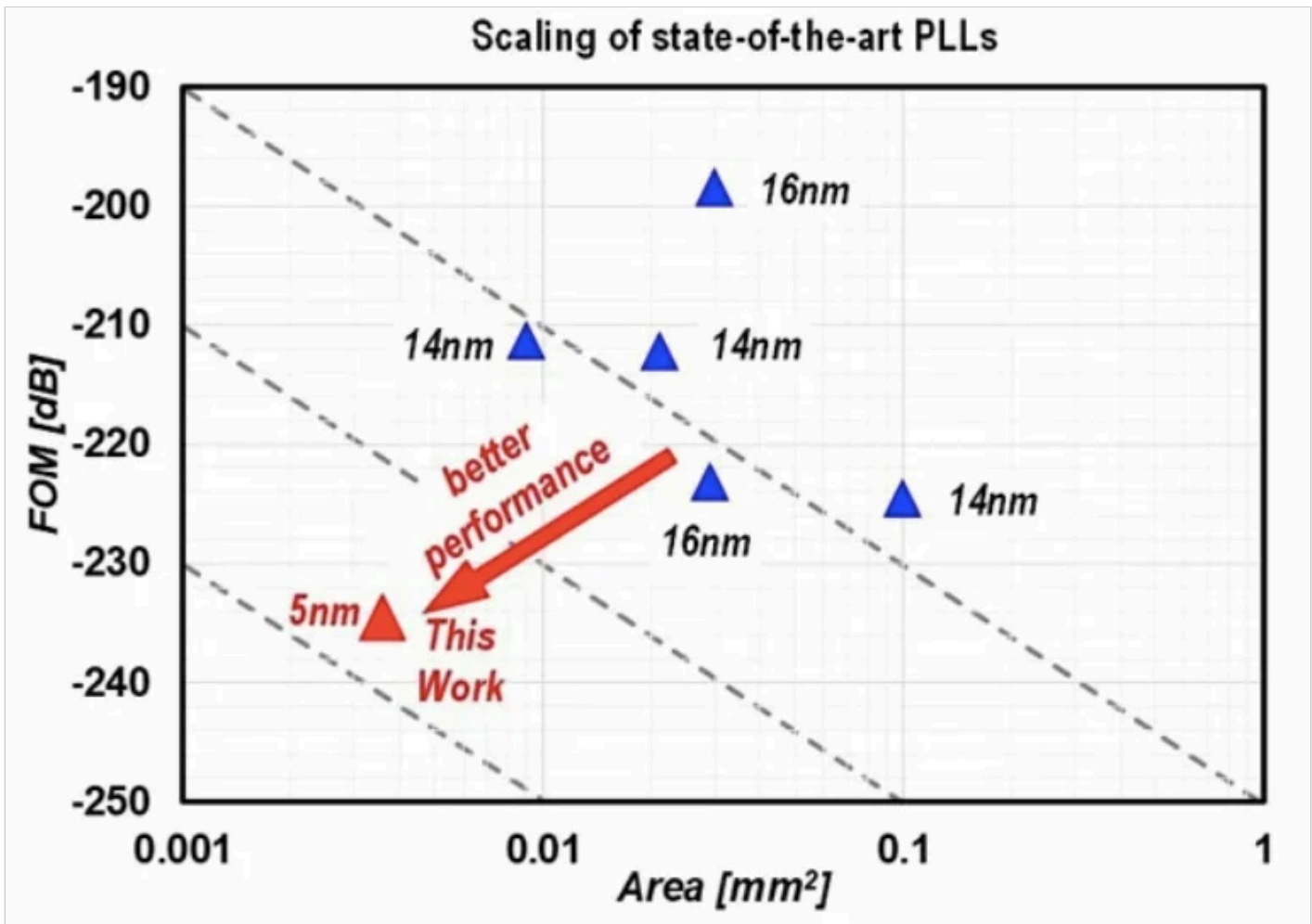
To reduce the area needed, the scientists used a ring oscillator, one of which can be easily scaled down to the required size. To dampen its phase noise, they used injection locking- processes of synchronizing an oscillator with an external signal whose frequency or multiple is close to that of the oscillator, which was done over a wide range of frequencies.

The reduction in jitter also carries the added benefit of reduced power consumption, making it an efficient design.

Better Size, Better Performance

The new design of the synthesizable PLL offers better performance, power consumption, and area size than anything currently on the market.

The scientists state in a [recently published paper on IEEE](#), “The PLL core area is 0.0036 mm². With 100-MHz reference frequency, better than -234.7 dB figure-of-merit (FOM) is achieved in the fractional-N mode, with -44.3 dBc worst-case fractional spur. The proposed PLL has the smallest chip area, highest FOM, and lowest fractional spur among ring oscillator (RO)-based fractional-N PLLs in sub-20-nm processes.”

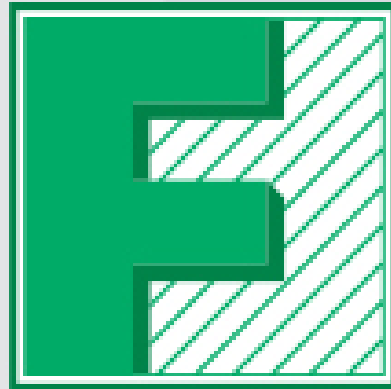


Comparison of FOM and area of PLLs in sub-20 nm CMOS processes. Image used courtesy of [Tokyo Tech News](#)

As mentioned earlier, the new PLLs can be easily integrated into future designs of all-digital processors. It's also commercially applicable, making it valuable for developing cutting-edge applications, including AI/machine learning, IoT, 5G cellular, and a host of others.

Both Tokyo Tech and Socionext plan to continue their partnership to advance the miniaturization of electronics, furthering the advancements to bring about tomorrow's technology.

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